(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 April 2004 (22.04.2004)

PCT

(10) International Publication Number
WO 2004/034631 A1

(51) International Patent Classification[7]: H04L 7/033

(21) International Application Number:
PCT/EP2002/011366

(22) International Filing Date: 10 October 2002 (10.10.2002)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant (*for all designated States except US*): INFINEON TECHNOLOGIES AG [DE/DE]; St.-Martin-Strasse 53, 81669 Munich (DE).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): SANDERS, Anthony [GB/DE]; Hugo Weiss Strasse 13, 81827 Munich (DE). PRETE, Edoardo [IT/DE]; Innere Wiener Strasse 16, 81667 Munich (DE).

(74) Agent: CHARLES, Glyndwr, Reinhard, Skuhra, Weise & Partner GbR, Friedrichstrasse 31, 80801 Munich (DE)

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

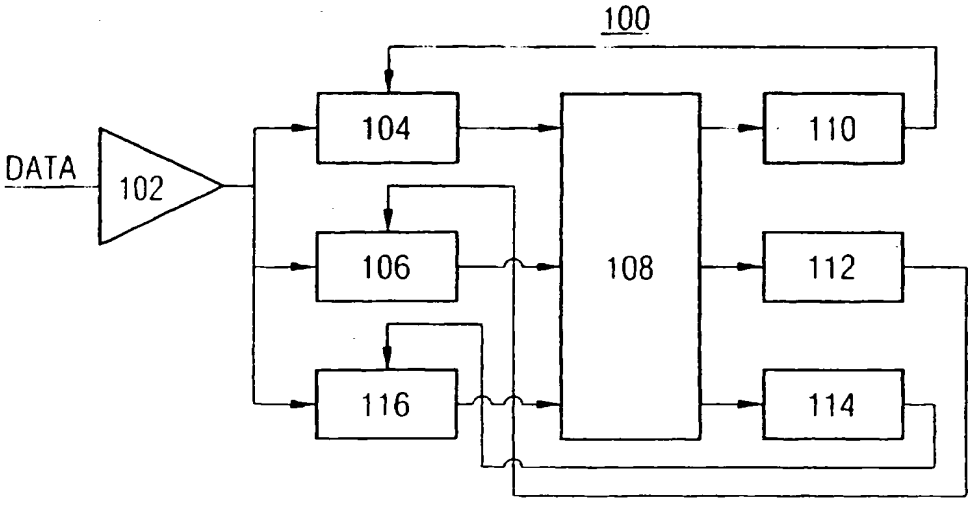
(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

For two letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CLOCK SIGNAL EXTRACTION DEVICE AND METHOD FOR EXTRACTING A CLOCK SIGNAL FROM A DATA SIGNAL



(57) Abstract: The invention provides a clock signal extraction device for extracting a clock signal from a periodic data signal, comprising a phase detector (104, 106) for detecting a first phase difference between rising edges of said data signal and a rising edges clock signal and for detecting a second phase difference between falling edges of said data signal and a falling edges clock signal; and a clock generator (110, 112) for generating said rising edges clock signal so that said first phase difference is minimized, for generating said falling edges clock signal so that said second phase difference is minimized, and for generating said clock signal in dependence on said first phase difference and said second phase difference. The invention further provides a method for extracting a clock signal from a periodic data signal.

WO 2004/034631 A1

Description

Clock Signal Extraction Device and Method for Extracting A Clock Signal from a Data Signal

The present invention relates to the extraction of a clock signal and data from a data signal in a digital communication system, e.g. an optical data signal in an optical communication system. In particular, the invention relates to a clock signal extraction device and a method for extracting a clock signal from a data signal.

Serial communication systems require the extraction of a sampling clock from a serial stream, where the clock harmonic is not intrinsic in the signal itself. This extraction is performed by a non-linear circuit called a Clock and Data Recovery (CDR) unit. The CDR is responsible for tracking low frequency phase changes in the signal by observing the transitions of the signal and performing averaging.

Fig. 2 illustrates a typical clock and data recovery (CDR) circuit 200 for recovering a clock signal and data from a data signal using a phase-locked loop (PLL). The CDR circuit 200 comprises a phase detector 202 which generates up or down pulses whose durations are proportional to the phase error between the recovered clock signal and the data signal. Outputs of the phase detector 202 are connected to a phase pump (charge pump) 204. The phase pump 204 is connected by a loop filter 206 to a voltage-controlled oscillator (VCO) 208 for charging the voltage-controlled oscillator 208 either "up" or "down" by a control voltage. This allows phase corrections of the clock signal provided by the voltage-controlled oscillator 208. The clock signal of the voltage-

controlled oscillator 208 is fed back to a clock input of the phase detector 202 forming the phase-locked loop. The clock signal or the recovered clock signal is also fed back to a clock input of a data sampler 210 for sampling the data signal at the rate of the recovered clock signal and for providing recovered data at a data output thereof. The recovered clock signal is a timing signal generated synchronous to the rate at which the original data pulses were transmitted from a transmitter in a communication system. The data sampler 210 preferably comprises a D-type flip-flop with a data input, a clock input and a data output. The phase detector preferably also comprises D-type flip-flops.

For example, in an optical communication system, a CDR is designed to find a mean phase of the transitions between low and high levels of an optical signal based on long-term averaging of the transitions. Fig. 3 shows an example of the superposition of transmitted data signals 302, 304 received at a receiver of the communication system and having ideal transition characteristics and undistorted amplitudes yielding to a perfect crossover of the signals. Broken curves 302', 304' further illustrate the effect of jitter 306 e.g. clock or phase jitter on the transition behaviour of the signals. For detecting the transition of a signal from a high state to a low state or vice versa, the transitions are sampled at a decision level in the middle of an eye formed by the superposed signals. The lower half of Fig. 3 shows the Probability Distribution Function (PDF) 308 of detected transitions of signals which are subjected to jitter. From this distribution, the mean transition value of the detected transitions is easily derived to obtain a mean sampling point for the sampling of data contained in a data signal.

However, in a long-haul optical communication system, signal distortion leads to an eye of the received data signal that is not optimal for a CDR. The distortion of the optical signals is caused e.g. by the optical dispersion of a transmission fibre and by the switch on/switch off behaviour of a transmitter like a laser.

Fig. 4 shows an example of the superposition of distorted optical signals 402, 404. The crossover of the falling and the rising edges of the signals is no longer positioned in the middle of a peak-to-peak amplitude of the eye, but towards the zero level of the optical signal. In such a case, the probability distribution function 408 of the detected transitions using a decision level in the middle of the eye comprises two peaks. Each peak is associated to the jittered transition of a falling edge and to the jittered transition of a rising edge of a signal, respectively. The jitter is shown at 406. It is readily visible that here the determination of a mean transition value is not possible. Rather, the distribution of the transitions leads to a dead zone, where the CDR is no longer able to find the mean transition value of the data signal. Since the sampling of the data from the data signal is based on a correct predict of the mean transition value, an unstable phase value will lead to a wrong sample of the data eye, thus leading to a degradation in the bit error rate of the link.

Usually, only averaging the transitions of either the rising or the falling edge of a signal solves this problem. Now that only a single edge is detected, the probability distribution function no longer has a dead zone and shows the same distribution as a signal, wherein the decision level is

positioned at the crossover. However, this method suffers from a reduction in the amount of phase error information provided to a phase-locked loop. As stated above, a CDR must track low-frequency wander, and its ability to achieve this is a function of the amount of phase error information available. By only using one edge of the data, half the information available to the CDR is lost, thus leading to a degradation of the tracking ability and an increase in the bit error rate of a receiver.

Fig. 5 shows another usual solution of the above problem in which the decision level of the CDR is simply adjusted to be at the crossover of the superposed data signals 502, 504. However, this solution suffers from the reduced signal-to-noise ratio of the transition amplitude, leading to false detection of transitions and false tracking of the signal. The reduced signal-to-noise ratio (S/N) is caused by the fact that due to the distortion of the signals, the crossover of the signals lies close to the low signal level which is strongly subjected to noise.

An object of the present invention is to provide a clock signal extraction device and a method for extracting a clock signal from a periodic data signal which enable the accurate determination of a mean transition value of a data signal and enable the reduction of the bit error rate in data transmission systems.

This object is achieved by a clock signal extraction device for extracting a clock signal from a periodic data signal according to claim 1 and a method for extracting a clock signal from a periodic data signal according to claim 11.

The basic idea of the invention is to use both edges of a data signal received at a receiver by individually averaging the probability distribution functions (see Fig. 4) of the rising and falling edges of the data signal using two independent phase-locked loops.

The invention relates to a clock signal extraction device for extracting a clock signal from a periodic data signal comprising a phase detector for detecting a first phase difference between rising edges of the data signal and a rising edges clock signal and for detecting a second phase difference between falling edges of the data signal and a falling edges clock signal; and a clock generator for generating the rising edges clock signal so that the first phase difference is minimized, for generating the falling edges clock signal so that the second phase difference is minimized, and for generating the clock signal in dependence on the first phase difference and the second phase difference.

The invention further relates to a method for extracting a clock signal from a periodic data signal, comprising detecting a first phase difference between rising edges of the data signal and a rising edges clock signal and detecting a second phase difference between falling edges of the data signal and a falling edges clock signal; and generating the rising edges clock signal so that the first phase difference is minimized, generating the falling edges clock signal so that the second phase difference is minimized, and generating the clock signal in dependence on the first phase difference and the second phase difference.

In the dependent claims advantageous developments and improvements of the device according to claim 1 and the method according to claim 11 are found.

According to a preferred development of the device according to the invention the clock generator generates the clock signal based on an average of the first phase difference and the second phase difference.

According to a further development of the device the clock generator comprises a first clock generator for generating the rising edges clock signal; a second clock generator for generating the falling edges clock signal; a third clock generator for generating the clock signal; and a controller for processing the first phase difference and the second phase difference and for controlling the first, second and third clock generator.

According to a further development of the device the phase detector comprises a first phase detector for detecting the first phase difference between the rising edges of the data signal and the rising edges clock signal; and a second phase detector for detecting the second phase difference between the falling edges of the data signal and the falling edges clock signal.

According to a further development of the device each of the first, second, and third clock generators comprises a voltage-controlled oscillator.

According to a further development of the device the controller comprises a phase pump and a loop filter.

According to a further development of the device the device is used in a data extraction device for extracting data from the data signal according to a rate of the clock signal.

According to a further development of the device the controller controls the clock generator for generating the clock signal such that the error rate of the extracted data is minimized.

According to a further development of the device the data extraction device comprises a data sampler for sampling the data signal.

According to a further development of the device the data sampler comprises a D-type flip-flop.

According to a development of the method according to the invention the step of generating comprises generating the clock signal based on an average of the first phase difference and the second phase difference.

According to a further development of the method the step of generating further comprises processing the first phase difference and the second phase difference; and generating and controlling the rising edges clock signal, the falling edges clock signal, and the clock signal.

According to a further development of the method the method further comprises extracting data from the data signal according to a rate of the clock signal.

According to a further development of the method the step of generating further comprises generating the clock signal such that the error rate of the extracted data is minimized.

According to a further development of the device and method according to the present invention the data signal is an optical data signal.

Preferred embodiments of the present invention are shown in the accompanying drawings, in which:

Fig. 1 shows a preferred embodiment of a device according to the invention;

Fig. 2 shows a typical clock and data recovery circuit;

Fig. 3 depicts a superposition of received signals having ideal transition characteristics in a communications system;

Fig. 4 depicts a superposition of distorted received signals in an optical communications system; and

Fig. 5 depicts a superposition of distorted received signals using a decision level at signal crossover for transition detection.

Fig. 1 shows a data extraction device 100 for extracting data from a data signal according to a rate of an extracted clock signal. The data extraction device 100 comprises a preferred embodiment of a clock signal extraction device for extracting the clock signal from the periodic data signal according to the invention. The clock signal extraction device uses phase informations from a rising edge and a falling edge of the

received data signal to generate tracking instructions provided to independent clock generators or phase generators.

The clock signal extraction device according to the invention comprises a receiver 102 for receiving a data signal received from a communication link of a communication system. The clock signal is preferably an optical baseband data signal received from an optical communication link, e.g. from an optical fibre of an optical communication system. The optical communication system is preferably a SONET (= Synchronous Optical NETwork) system.

The clock signal extraction device further comprises a first phase detector 104 and a second phase detector 106 connected with a respective input thereof to an output of the receiver 102, a controller 108 connected with respective inputs thereof to a respective output of the first phase detector 104 and the second phase detector 106, and a first clock generator 110, a second clock generator 112 and a third clock generator 114 connected with respective inputs thereof to respective outputs of the controller 108. The first clock generator 110 comprises an output connected to a further input of the first phase detector 104 forming a first loop. The second clock generator 112 comprises an output connected to a further input of the second phase detector 106 forming a second loop.

The first phase detector 104 detects a first phase difference between the transitions of rising edges or detection points of rising edges of the data signal and a rising edges clock signal generated by the first clock generator 110. The second phase detector 106 detects a second phase difference between the transitions of falling edges or detection points of

falling edges of the data signal and a falling edges clock signal generated by the second clock generator 112. The first, second, and third clock generators 110, 112, and 114 preferably comprise a voltage-controlled oscillator (VCO).

The controller 108 processes the first phase difference provided by the first phase detector 104 and the second phase difference provided by the second phase detector 106 and controls the first clock generator 110 and the second clock generator 112 so that the first and second phase differences are minimized. Furthermore, the controller 108 controls the third clock generator 114 for generating an extracted clock signal in dependence on the first and second phase differences. The controller preferably controls the third clock generator in dependence on an average of the first phase difference and the second phase difference. The controller 108 preferably comprises a phase pump and a loop filter associated to each first, second and third clock generator 110, 112 and 114.

Further to the clock signal extraction device the data extraction device 100 comprises a data sampler 116 connected to the output of the receiver 102, to an output of the third clock generator 114 for receiving the extracted clock signal, and to a further input of the controller 108. The data sampler 116 preferably comprises a D-type flip-flop controlled by the extracted clock signal for sampling the data signal and extracting the data accordingly.

In another embodiment of the invention, the controller 108 further controls the third clock generator in dependence on a phase difference supplied to the controller 108 by the data sampler 116. In a even further embodiment of the invention,

the controller 108 controls the third clock generator 114 such that the error rate of the extracted data is minimized.

In a method according to the present invention, a clock signal is extracted from a periodic data signal. In a first step of the method, a first phase difference between rising edges of a data signal and a rising edges clock signal is detected and a second phase difference between falling edges of a data signal and a falling clock signal is detected. In a second step of the method, the rising edges clock signal is generated such that the first phase difference is minimized, and the falling edges clock signal is generated such that the second phase difference is minimized, and the clock signal is generated in dependence on the first phase difference and the second phase difference. The clock signals are preferably generated based on an average of the first phase difference and the second phase difference. In a further step of the invention, data is extracted from a data signal according to a rate of the extracted clock signal. The clock signal is preferably generated such that the error rate of the extracted data is minimized. The method of the invention is preferably implemented in a digital signal processor (DSP).

One advantage of the present invention is that by individually finding the mean transition value of a data signal, there is no longer any dead zone. The individual mean transition values of the rising and falling edges of the data signal can be used to define the ideal sampling point of a received data eye such that the data samples have the lowest possible error rate.

List of reference signs

Fig. 1

100 data extraction device
102 receiver
104 first phase detector
106 second phase detector
108 controller
110 first clock generator
112 second clock generator
114 third clock generator
116 data sampler

Fig. 2
200 clock and data recovery circuit
202 phase detector
204 phase pump
206 loop filter
208 voltage-controlled oscillator
210 data sampler

Claims

1. A clock signal extraction device for extracting a clock signal from a periodic data signal, comprising:
- a phase detector (104, 106) for detecting a first phase difference between rising edges of said data signal and a rising edges clock signal and for detecting a second phase difference between falling edges of said data signal and a falling edges clock signal; and
- a clock generator (110, 112) for generating said rising edges clock signal so that said first phase difference is minimized, for generating said falling edges clock signal so that said second phase difference is minimized, and for generating said clock signal in dependence on said first phase difference and said second phase difference.

2. The device according to claim 1,
characterized in that
said clock generator (104, 106) generates said clock signal based on an average of said first phase difference and said second phase difference.

3. The device according to claim 1 or 2,
characterized in that
said clock generator comprises:
- a first clock generator (110) for generating said rising edges clock signal;
- a second clock generator (112) for generating said falling edges clock signal;
- a third clock generator (114) for generating said clock signal; and
- a controller (108) for processing said first phase difference and said second phase difference and for

controlling said first, second and third clock generator (110, 112, 114).

4. The device according to claim 1, 2 or 3,
characterized in that
said phase detector comprises:
- a first phase detector (104) for detecting said first phase difference between said rising edges of said data signal and said rising edges clock signal; and
- a second phase detector (106) for detecting said second phase difference between said falling edges of said data signal and said falling edges clock signal.

5. The device according to claim 3 or 4,
characterized in that
each of said first, second and third clock generators (110, 112, 114) comprises a voltage controlled oscillator.

6. The device according to claim 3, 4 or 5,
characterized in that
said controller (108) comprises a phase pump and a loop filter.

7. The device according to one of the preceding claims,
characterized in that
said device is used in a data extraction device (100) for extracting data from said data signal according to a rate of said clock signal.

8. The device according to claim 7,
characterized in that

said controller (108) controls said clock generator (110, 112, 114) for generating said clock signal such that the error rate of the extracted data is minimized.

9. The device according to claim 7 or 8,
characterized in that
said data extraction device (100) comprises a data sampler (116) for sampling said data signal.

10. The device according to claim 9,
characterized in that
said data sampler (116) comprises a D-type flip-flop.

11. A method for extracting a clock signal from a periodic data signal, comprising:
- detecting a first phase difference between rising edges of said data signal and a rising edges clock signal and detecting a second phase difference between falling edges of said data signal and a falling edges clock signal; and
- generating said rising edges clock signal so that said first phase difference is minimized, generating said falling edges clock signal so that said second phase difference is minimized, and generating said clock signal in dependence on said first phase difference and said second phase difference.

12. The method to claim 11,
characterized in that
said step of generating comprises generating said clock signal based on an average of said first phase difference and said second phase difference.

13. The method according to claim 11 or 12,
characterized in that

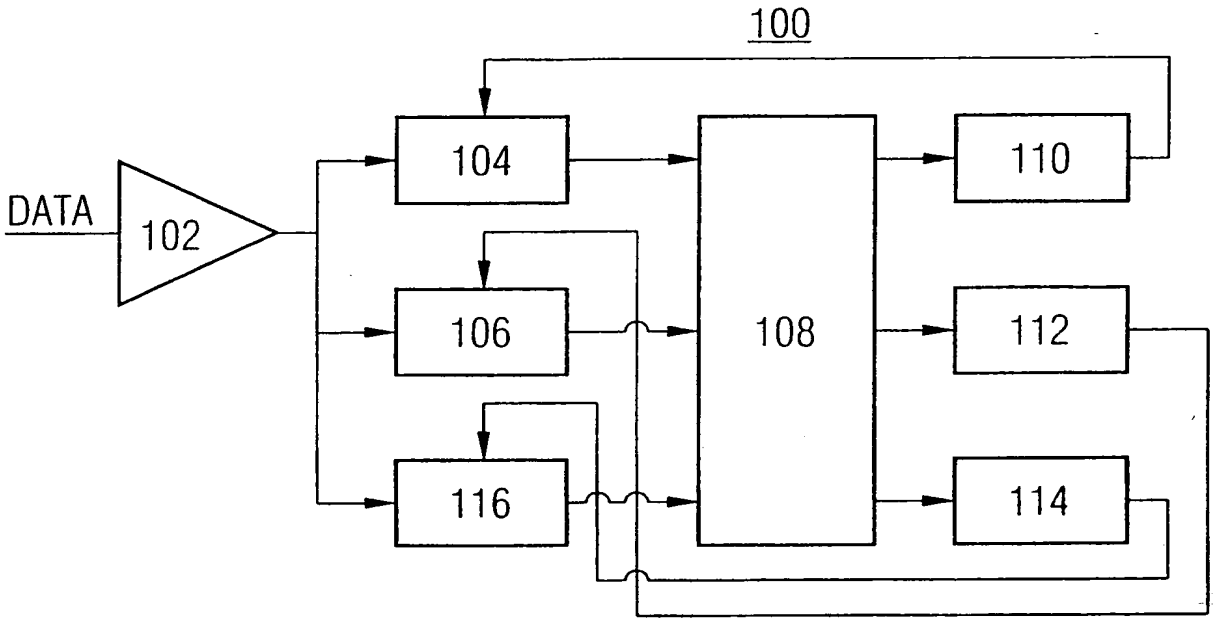
said step of generating further comprises:
- processing said first phase difference and said second phase difference; and
- generating and controlling said rising edges clock signal, said falling edges clock signal, and said clock signal.

14. The method according to claims 11 to 13,
c h a r a c t e r i z e d i n t h a t
said method further comprises:
- extracting data from said data signal according to a rate of said clock signal.

15. The method according to claim 14,
c h a r a c t e r i z e d i n t h a t
said step of generating further comprises generating said clock signal such that the error rate of said extracted data is minimized.

16. The device or the method according to one of the preceding claims,
c h a r a c t e r i z e d i n t h a t
said data signal is an optical data signal.

FIG 1



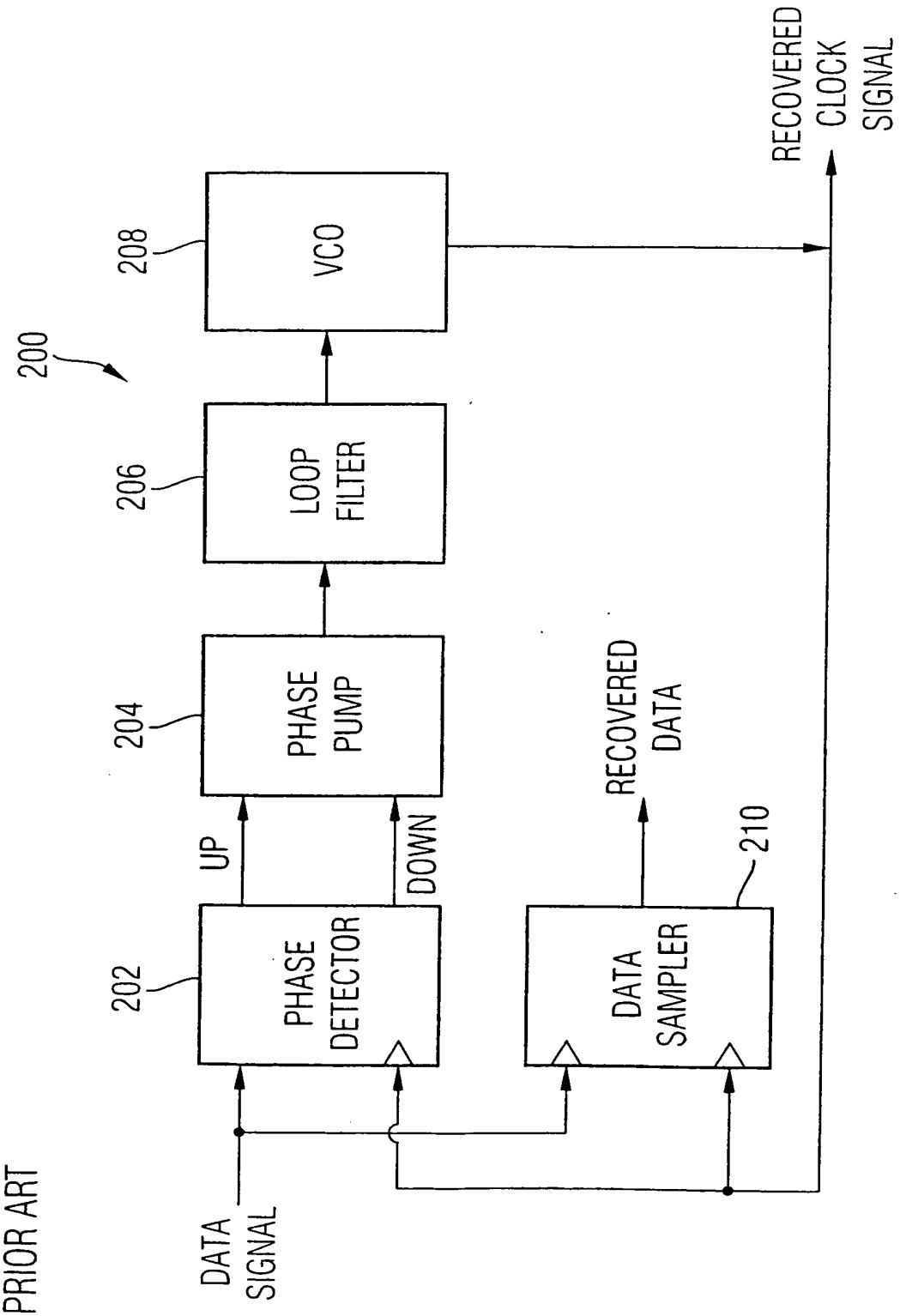


FIG 2
PRIOR ART

FIG 3

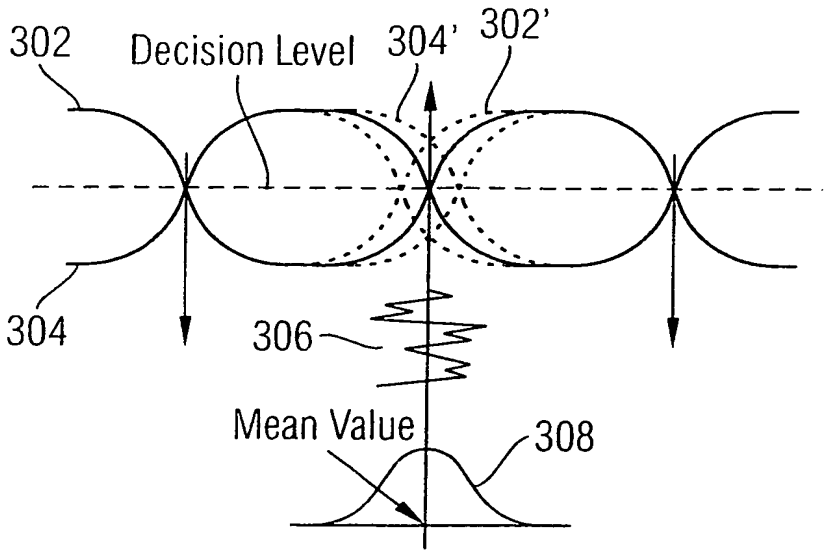


FIG 4

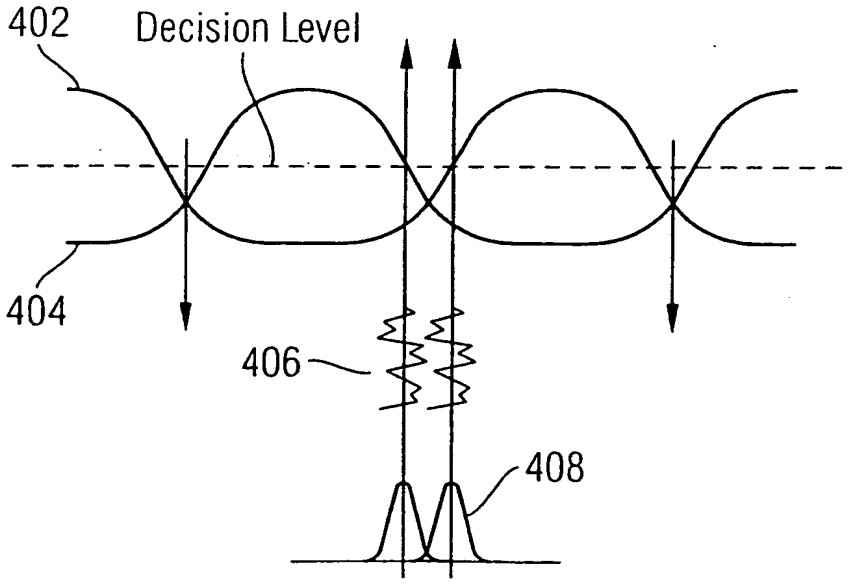
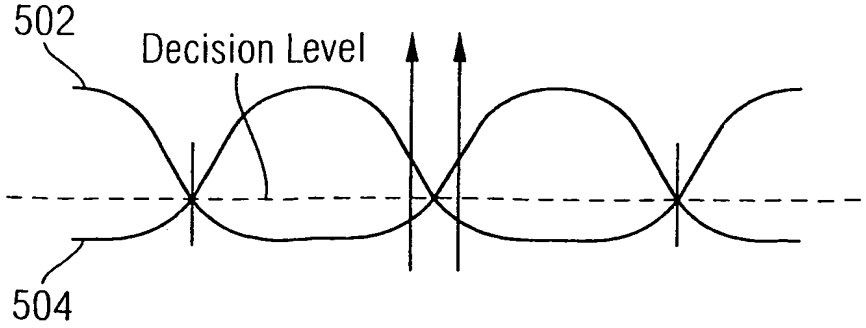


FIG 5



INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 02/11366

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L7/033

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04L H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, PAJ, IBM-TDB, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 713 802 A (KOBATA HIROSHI ET AL) 15 December 1987 (1987-12-15) column 1, line 22 - line 45 column 2, line 20 - line 32 column 3, line 21 -column 4, line 18 figure 3	1,3-11, 13-16
Y	---	2,12
Y	US 6 236 696 B1 (BABA MITSUO ET AL) 22 May 2001 (2001-05-22) column 4, line 11 - line 40 figure 1	2,12

A	US 6 166 606 A (TSYRGANOVICH ANATOLIY V) 26 December 2000 (2000-12-26) column 3, line 63 - line 66 column 7, line 2 - line 6 figure 4	2,12

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 May 2003	05/06/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Baltersee, J

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern[illegible]pplication No
PCT/EP 02/11366

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4713802 A	15-12-1987	JP 61227269 A	09-10-1986
		JP 61227270 A	09-10-1986
		JP 61227271 A	09-10-1986
		DE 3672003 D1	19-07-1990
		EP 0200370 A1	05-11-1986
		KR 9001593 B1	15-03-1990
US 6236696 B1	22-05-2001	JP 3072833 B2	07-08-2000
		JP 10327068 A	08-12-1998
US 6166606 A	26-12-2000	NONE	